UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/994,233	11/26/2001	Michael A. Nix	X-1012 US	8295

24309 7590 04/18/2003

XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER
NGUYEN, LONG T

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

Office Action Summary	Application No.	Applicant(s)
	09/994,233	NIX, MICHAEL A.
	Examiner	Art Unit
	Long Nguyen	2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 January 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. The amendment filed on 1/8/03 has been received and entered in the case.

Claim Objections

2. Claims 11 and 17 are objected to because of the following informalities:

Claim 11, line 2, "further" should be deleted.

Claim 17, line 6, "and" should be deleted.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Ooishi (JP 2000244287).

With respect to claim 1, Figure 9 of the Ooishi reference discloses a flip-flop circuit which includes: a differential output stage (23, and transistors NG3-NG4 in 24) having differential first and second input terminals (D3 and /D3) and complementary first and second output terminals (nodes OD4 and OD3); a transistor (NT3) having a first current-handling terminal connected to the first output terminal (OD4), a second current-handling terminal connected to the second output terminal (OD3), and a control terminal (gate); and a cross-coupled circuit (PQ3-PQ4, NQ3-NQ4, PQ6) having a cross coupled transistor (NQ4) directly

connected to a power supply voltage (NS1), wherein a gate of the cross-coupled transistor (NQ4) is connected to the second output terminal (OD3).

With respect to claim 2, Figure 9 shows a clock terminal (TG2) connected to the control terminal (gate of transistor NT3 connected to receiving clock TG2).

With respect to claim 3, Figure 9 shows a second transistor (n-channel transistor of transmission gate CQ1) having a third current-handling terminal connected to the first input terminal (D3), a fourth current-handling terminal connected to the second input terminal (/D3), and a second control terminal (gate).

With respect to claim 4, Figure 9 of the Ooishi reference includes a first clock terminal (TG2) connected to the first-mentioned control terminal (gate of transistor NT3 connected to receive clock signal TG2) and a second clock terminal (TG1) connected to the second control terminal (gate of n-channel transistor of transmission gate CQ1 connected to receive clock TG1). Note that the Examiner treats this claim as if it depends on claim 3.

With respect to claim 5, the limitation "the first and second clock terminals are adapted to receive complementary clock signals" is met because clocks TG2 and TG1 are complementary clock signals (see Figure 10).

With respect to claim 6, Figure 9 of the Ooishi reference shows that the flip-flop circuit includes a differential input stage (21-22) having differential third and fourth input terminals (D and /D) and complementary third and fourth output terminals (nodes OD2 and OD1) connected to the first and second input terminals (D3 and D3/), respectively.

With respect to claim 7, Figure 9 shows a clock terminal (TG2) connected to the control terminal (gate of transistor NT3 connected to receive clock signal TG2).

With respect to claim 8, Figure 9 shows a second transistor (n-channel transistor of transmission gate CQ1) having a third current-handling terminal connected to the first input terminal (D3), a fourth current-handling terminal connected to the second input terminal (/D3), and a second control terminal (gate of n-channel transistor of transmission gate CQ1).

With respect to claim 9, Figure 9 shows the control terminal (gate of NT3) and the second control terminal (gate of the n-channel transistor of transmission gate CQ1) are adapted to receive complementary clock signals (TG2 and TG1 are complementary clock signals, see Figure 10).

5. Claims 10-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Hwang et al. (USP 5,777,491).

With respect to claim 10, Figure 1 of the Hwang et al. reference discloses a circuit, which includes: a differential input stage (11, 12) having differential first and second input terminals (BN, B), differential third and fourth input terminals (AN, A), a first transistor (N3), and complementary first and second output terminals (Q, QN), wherein the first transistor (N3) has a first control terminal (gate) connected to the first input terminal (BN) and a current handing terminal (source of N3) directly connected to VSS (ground).

With respect to claim 11, Figure 1 of the Hwang et al. reference shows that the input stage (11, 12) includes a first leg (12) including the first transistor (N3) and a second transistor (N4) connected in parallel, the second transistor (N4) having a second control terminal (gate) connected to the third input terminal (AN).

With respect to claim 12, Figure 1 of the Hwang et al. reference shows that the input stage (11, 12) includes a second leg (12) having third and fourth transistors (N2, N1) connected

in series, the third transistor (N2) having a third control signal (gate) connected to the second input terminal (B) and the fourth transistor (N1) having a fourth control terminal (gate) connected to the fourth input terminal (A).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hwang et al. (USP 5,777,491) in view of Choe (USP 6,373,292).

With respect to claim 13, Figure 1 of the Hwang et al. reference discloses a circuit (as discussed above with regard to claims 10-13) includes all of the limitations of this claim except for a transistor having a first current-handling terminal connected to the first output terminal of the differential input stage, a second current-handling terminal connected to the second output terminal of the differential input stage, and a control terminal. However, Figure 2 of the Choe reference discloses a differential circuit which includes a transistor (56) having a control terminal (gate), a first current-handling terminal connected to the first output terminal (OUT) and a second current-handling terminal connected to the second output terminal (OUT/) for the purpose of reducing power consumption and improving the speed of the circuitry (line 25 of Col. 2 to line 10 of Col. 3). It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the circuit in Figure 1 of the Hwang et al. reference with a transistor connected between the output terminals (i.e., a transistor connected between outputs

Q and QN in Figure 1 of the Hwang et al. reference) as taught by the Choe reference for the purpose of reducing power consumption and improving the speed of the circuitry.

With respect to claim 14, the above combination meets the limitation of a clock terminal connected to the control terminal (i.e., a clock signal is connected the gate of the transistor that has the first and second current-handling terminals connected to outputs Q and QN, respectively).

8. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choe (USP 6,373,292) in view of Hwang et al. (USP 5,777,491).

With respect to claim 15, Figure 2 of the Choe reference discloses a circuit (40) which includes an output stage (40), wherein the output stage (40) receiving a differential input signal (In, In/). Figure 2 of the Choe reference does not specially disclose how the differential input signal (In, In/) is generated. However, Figure 1 of the Hwang et al. reference discloses an input stage circuit that generate differential signal (Q, QN) for the purpose of low power dissipation and requires only a small chip area for fabrication (see Col. 2, lines 1-8 of the Hwang et al. reference). It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the circuit in Figure 1 of the Hwang et al. reference to provide the differential signal (Q, QN) to the differential input (In, In/) of the circuit in Figure 2 of the Choe reference (i.e., signals Q and QN in Figure 1 of the Hwang et al. reference are respectively to signals In and In/ in Figure 2 of the Choe et al. reference) for the purpose of low power dissipation and requires only a small chip area for fabrication (see Col. 2, lines 1-8 of the Hwang et al. reference). Thus, this combination meets all the limitation of claim 15, i.e., the above combination includes an input stage (Figure 1 of the Hwang et al. reference) including a

differential input stage (11, 12) having differential first and second input terminals (BN, B), differential third and fourth input terminals (AN, A), a first transistor (N3), and complementary first and second output terminals (Q, QN), wherein the first transistor (N3) has a first control terminal (gate) connected to the first input terminal (BN) and a current handing terminal (source of N3) directly connected to VSS (ground); an output stage (Figure 2 of the Choe reference) including differential fifth and sixth input terminals (In and In/, Figure 2 of Choe) connected to respective ones of the first and second output terminals (Q and QN of Hwang et al.), complementary third and fourth output terminals (OUT and OUT/ in Figure 2 of Choe), and a transistor (56, Figure 2 of Choe) having a control terminal (gate), a first current-handling terminal (64, Figure 2 of Choe) connected to the third output terminal (OUT, Figure 2 of Choe) and a second current-handling terminal (62, Figure 2 of Choe) connected to the fourth output terminal (OUT/, Figure 2 of Choe).

With respect to claim 16, Figure 2 of the Choe reference in the above combination also meets the limitation of a clock terminal (CLK/) connected to the control terminal (gate of transistor 56 in Figure 2 of Choe).

9. Claims 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (Figure 1) in view of Ooishi (JP 2000244287).

Applicant's admitted prior art (Figure 1) discloses a counter circuit which includes a first flip-flop (first flip-flop 110 from the left) having differential first and second outputs (Q and Q/ of the first flip-flop) and a second flip-flop (second flip-flop 110 from the left) having differential first and second inputs (D and D/ of the second flip-flop) wherein the differential first and second inputs of the second flip-flop are connected to receive the differential first and

second outputs of the first flip-flop, respectively, wherein the details of each flip-flop 110 in Figure 1 are shown in instant Figure 2 (prior art). Applicant's admitted prior art does not disclose that the first flip-flop includes a differential output stage having differential output stage, a first transistor, and a cross coupled circuit; and the second flip-flop includes a differential input stage, a second transistor, and a third transistor with the recited connections set forth in claim 17. However, Figure 9 of the Ooishi reference discloses a flip-flop circuit which operates at high-speed and low current consumption (see Col. 17, lines 42-57 of US Patent 6,433,586 which is the English version of the JP 2000244287 reference) which includes: a differential output stage (23, and transistors NG3-NG4 in 24) having differential first and second input terminals (D3 and /D3) and complementary first and second output terminals (OQ and /OQ), a first transistor (NT3) having a first control terminal (gate of NT3), a first current-handling terminal connected to the first output terminal (OQ by way of inverter 25a) and a second current-handling terminal connected to the second output terminal (/OQ by way of inverter 25b), and a cross-coupled circuit (PQ3-PQ4, NQ3-NQ4, PQ6) having a cross coupled transistor (NQ3) directly connected to a power supply voltage (NS1), wherein a gate of the cross-coupled transistor (NQ3) is connected to the second output terminal (/OQ, by way of inverter 25b); and a differential input stage (21-22 except transmission gate CQ1 in 22) having differential third and fourth input terminals (D and /D) and complementary third and fourth output terminals (nodes OD2 and OD1) connected to the first and second input terminals (D3 and D3/) of the differential output stage, respectively, a second transistor (NT2) having a gate connected to the third input terminal (D, by way of transistor 21a) and a current handling terminal (source of transistor NT2) directly connected to VSS (ground); and a third transistor (the n-channel transistor of transmission gate

CQ1) having a second control terminal (gate) and third and fourth current-handling terminals connected to the third and fourth output terminals (nodes OD2 and OD1), respectively. It would have been obvious to one having ordinary skill in the art at the time the invention was made to replace each of flip-flops 110 in Figure 1 of applicant's admitted prior art (the details of each flip-flop are shown in Figure 2) with the flip-flop shown in Figure 9 of the Ooishi reference for the purpose of reducing the current consumption of the circuitry and operating the circuitry at high-speed. Thus, based on this combination, all of the limitations recited claim 17 are met.

With respect to claim 18, the above combination meets the limitation "the first and second control terminals are adapted to receive complementary clock signals" recited in this claim because clocks signals TG2 and TG1 are complementary clock signals (see Figure 10).

With respect to claim 19, the first flip-flop (the first flip-flop from the left in the above combination) includes a second differential input stage (i.e., 21-22 in Figure 9 of the Ooishi reference) having differential fifth and sixth input terminals (D and D/ in Figure 9 of the Ooishi reference) and complementary fifth and sixth output terminals (nodes OD2 and OD1 in Figure 9 of the Ooishi reference), wherein the fifth and sixth output terminals (nodes OD2 and OD1) are connected to the first and second input terminals (D3 and /D3), respectively.

With respect to claim 20, the second flip-flop (the second flip-flop from the left in the above combination) includes a second differential output stage (23-25 in Figure 9 of the Ooishi reference) having differential fifth and sixth input terminals (D3 and /D3 in Figure 9) connected to the third and fourth output terminals (nodes OD2 and OD1 in Figure 9), respectively.

Response to Arguments

10. Applicant's arguments with respect to amended claims 1-20 have been considered but are moot in view of the new ground(s) of rejection as discussed above. Note that, for claims 1 and 17, Figure 9 of the Ooishi reference shows transistors NQ3 and NQ4 having their source directly connected to a power supply voltage (NS1, see lines 17-29 of Col. 17 in the Ooishi reference, USP 6,433,586), and transistors NT1-Nt2 having their source directly connected to ground.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (703) 308-6063. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (703) 308-4876. The fax number for this group is (703) 872-9318. The After Final fax number is (703) 872-9319.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is (703) 308-0956.

April 15, 2003

LN

Long Nguyen
Art Unit: 2816

Terry D. Cunningham
Primary Examiner